2. (Amended) A ferroelectric memory, comprising:

a substrate;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the substrate;

a microstructure; and

a peripheral circuit for the passive matrix array, the peripheral circuit being formed on the microstructure, the microstructure being integrated on the substrate.

3. (Amended) A ferroelectric memory, comprising:

a first microstructure;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the first microstructure;

a second microstructure;

a peripheral circuit for the passive matrix array, the peripheral circuit being formed on the second microstructure; and

a substrate, the first and second microstructures being integrated on the substrate.

4. (Amended) The ferroelectric memory according to claim 1, further including a plurality of microstructures integrated on the substrate.

5. (Amended) The ferroelectric memory according to claim 1, wherein:

a recess portion in which the microstructure is provided is formed in the substrate; and

the microstructure is provided in the recess portion and integrated on the substrate.

6. (Amended) The ferroelectric memory according to claim 5,

wherein the substrate is formed by transfer-molding a photocurable resin.

7. (Amended) A ferroelectric memory, comprising:

a first microstucture;

a plurality of pairs of a passive matrix array that each includes memory cells formed of ferroelectric capacitors, the plurality of pairs of the passive matrix array being provided on the first microstructure;

a second microstructure;

a peripheral circuit for the passive matrix array, the peripheral circuit being formed on the second microstructure; and

a substrate, at least one of the pairs of the passive matrix array being provided on each side of the substrate.

8. (Amended) A ferroelectric memory, comprising:

a passive matrix array that includes memory cells formed of ferroelectric capacitors;

a peripheral circuit for the passive matrix array;

an associated circuit having a same or a different function as the memory cells;

a single substrate; and

a plurality of microstructures, the passive matrix array, the peripheral circuit and the associated circuit being formed on each of the plurality of microstructures, the microstructures being integrated on the single substrate.

9. (Amended) A ferroelectric memory, comprising:

a passive matrix array that includes memory cells formed of ferroelectric capacitors;

a peripheral circuit for the passive matrix array; and

a single microstructure, the passive matrix array and the peripheral circuit being integrated on the single microstructure.

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10. (Amended) A ferroelectric memory, comprising:

Sub B2

a first microstructure;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the first microstructure;

a second microstructure that is larger than the first microstructure, the first microstructure being provided in a part of the second microstructure to be integrated; and

a peripheral circuit for the passive matrix array, the peripheral circuit being formed on the second microstructure.

11. (Amended) A ferroelectric memory, comprising:

a plurality of microstructures;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on each of the plurality of microstructures;

a peripheral circuit for the passive matrix array; and

a substrate, the microstructures being provided in layers to be integrated in the substrate.

12. (Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:

Sub B3

forming the passive matrix array on a microstructure;

forming the peripheral circuit on a substrate; and

integrating the microstructure on the substrate.

13. (Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:

forming the passive matrix array on a substrate;

forming the peripheral circuit on a microstructure; and

integrating the microstructure on the substrate.

14. (Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:

forming the passive matrix array on a first microstructure;

forming the peripheral circuit on a second microstructure; and

integrating the first and second microstructures on a substrate.

15. (Amended) The method of fabricating a ferroelectric memory according to claim 12, further including:

forming a recess portion in the substrate which corresponds to a shape of the microstructure; and

providing the microstructure in the corresponding recess portion in the substrate to be integrated.

16. (Amended) The method of fabricating a ferroelectric memory as defined in claim 15,

wherein the step of providing the microstructure includes providing a fluid which contains the microstructure to a surface of the substrate.

17. (Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:

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forming a plurality of pairs of the passive matrix array on a first microstructure;

forming the peripheral circuit on a second microstructure; and

integrating at least one of the pairs on each side of a substrate.

Sub B4

18. (Amended) A method of fabricating a ferroelectric memory, which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:

forming the passive matrix array on a first microstructure;

forming the peripheral circuit on a second microstructure which is larger than the first microstructure; and

providing the first microstructure in a part of the second microstructure to be integrated.

19. (Amended) A method of fabricating a ferroelectric memory, which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:

forming the passive matrix array on each of a plurality of microstructures; and

providing the microstructures in layers to be integrated in a substrate.

Please add new claims 20-25 as follows:

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--20. The ferroelectric memory according to claim 2, further including a plurality of microstructures integrated on the substrate.--

--21. The ferroelectric memory according to claim 2, wherein:

a recess portion in which the microstructure is provided is formed in the substrate; and

the microstructure is provided in the recess portion and integrated on the substrate.--

--22. The ferroelectric memory according to claim 3, further including a plurality of microstructures integrated on the substrate.--

--23. The ferroelectric memory according to claim 3, wherein:

a recess portion in which the microstructure is provided is formed in the substrate; and

the microstructure is provided in the recess portion and integrated on the substrate.--

--24. The method of fabricating a ferroelectric memory according to claim 13, further including:

forming a recess portion in the substrate which corresponds to a shape of the microstructure; and

providing the microstructure in the corresponding recess portion in the substrate to be integrated.--

--25. The method of fabricating a ferroelectric memory according to claim 14, further including:

forming a recess portion in the substrate which corresponds to a shape of the microstructure; and

providing the microstructure in the corresponding recess portion in the substrate to be integrated.--

REMARKS

Claims 1-25 are pending. By this Preliminary Amendment, claims 1-19 are amended, and claims 20-25 are added. The specification and Abstract are replaced with a Substitute Specification and Substitute Abstract.